Xp-Graphène (2009)

Growth, fabrication and electronic properties of epitaxial graphene

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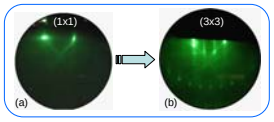
Collaboration: Small System lab, Georgiatech

Growth objectives and conditions

The direct growth of graphene has been achieved by molecular beam epitaxy (MBE), using a solid carbon source. Silicon carbide substrates have been used to reduce lattice mismatch problems.

(3x3) reconstruction generation



These two pictures show the SiC RHEED diagrams along the [12-30] direction. No particular surface reconstruction is observed during the whole surface preparation step (photo (a)). After ~20s exposure to the carbon flux at 1030°C, the (3x3) reconstruction appears on the SiC carbon face (photo (b)). It thus proves that the solid source flux generates an **atomic flux of carbon**. In comparison with the graphitization, the C-rich (3x3) reconstruction appears at higher temperature (>1100°C).

MBE growth chamber

Structural analysis

Graphene growth has been studied on both 6H-SiC faces : (0001) and (000-1).

AFM pictures (fig. 1) of SiC surfaces after Si flux exposure, Si face (a) and C face (b).

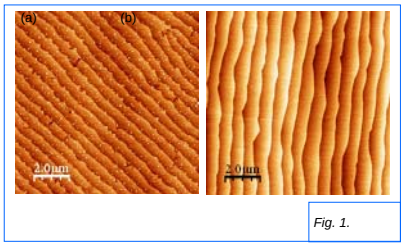


Fig. 1.

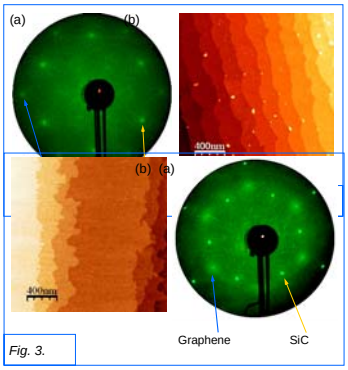


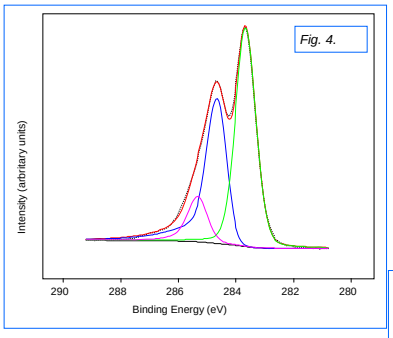
Fig. 3.

LEED diagrams (a) and AFM pictures (b) of graphene growth from carbon solid-source during **3 minutes at 1000°C on the silicon face** (fig. 2) and **4 minutes at 1035°C on the carbon face** (fig. 3).

The flat atomic steps remains unaffected during the formation of graphene because the temperature is below the one required for graphitization. LEED patterns confirm the presence of graphene on the surface (blue arrows).

XPS analysis

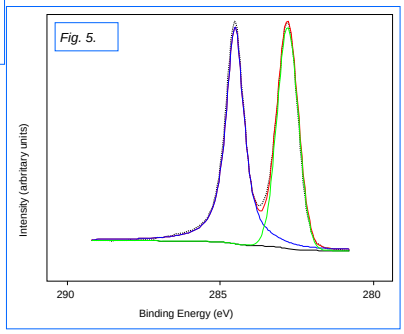
Figures 4 and 5 represent the XPS spectra of C1s for graphene grown on Si-face (3 minutes growth, c.f. fig. 2) and C-face (4 minutes growth, c.f. fig. 3) respectively. The thickness of graphene has been calculated from the attenuation of the substrate carbon atoms peak intensity by the graphene layers.



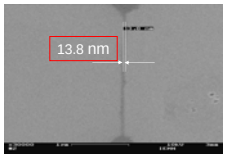
On SiC (0001) (fig. 4), three components corresponding to the bulk, interface and graphene are needed to fit the experimental curve. The average thickness was found to be **0.49±0.05 nm or about 1.5 ML** (Monolayer).

In the case of **SiC (000-1)** (fig. 5), only two components are required. The thickness calculation gives **0.69±0.07 nm i.e. 2.1 ML**.

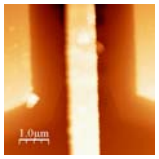
It must be emphasized that the XPS spectra (number and position of components) are nearly identical for graphene grown by MBE or graphitization.



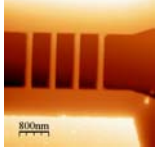
Graphene Nano Ribbon FET fabrication



Etched graphene

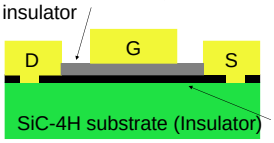


A top gated device



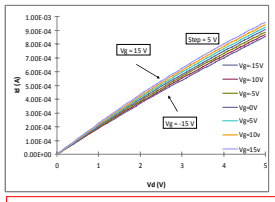
HSQ patterned multi-channels passive device

Oxidized HSQ as gate insulator



Graphene layer

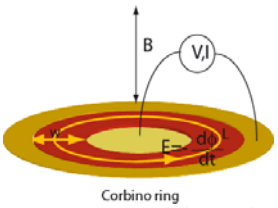
Illustration (side view) for a top gated device



First results for a 300 nm wide Graphene Nano Ribbon FET :

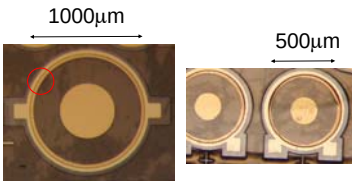
- G_m = 0.38 µS
- Dirac point at -18 V for our device
- No "OFF" state

Hall effect in Corbino geometry

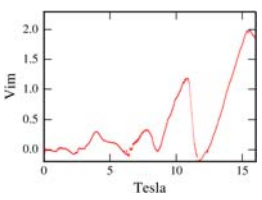


electrodes

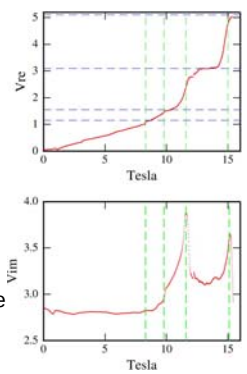
Corbino grahene rings on SiC



Recognizable QH plateaus



Dissipative peaks as LL sweeps through Fermi levels



Understand charge transfer between grahene Layers (how is the Fermi level pinned ?)